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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,347	02/27/2004	Hajime Kimura	12732-212001 / US7008	2831
26171	7590	09/26/2006	EXAMINER	
FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			NGUYEN, HIEP	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/787,347	Applicant(s) KIMURA, HAJIME	
	Examiner Hiep Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4,5,7-16 and 47-52 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 7-16,51 and 52 is/are allowed.
- 6) ☒ Claim(s) 1,2,4,5 and 47-50 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 September 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 4 and 47-50 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation “wherein... the second current to the load” on lines 9-11 is indefinite because it is misdescriptive. One of ordinary skill in the art knows that unlike a bipolar transistor, a MOS or a FET transistor does not have gate current because the gate is isolated from the body of the transistor. The “ON/OFF” depends on the polarity of the voltage applied to the gate. Thus; the “a first potential” or “a second potential” is the potential directly applied to the gate of the transistor. The “first potential” or the “second potential” is misdescriptive. The second current which flows through the load is not the “second current” is not the second current “fed” to the gate of the transistor. The recitation “wherein the transistor feeds the second current to the load” on line 12 is indefinite because it is not the “second current” on line 10 that is “fed” to the gate of the transistor. The same rationale is applied to claims 2 and 4.

Regarding claims 4, 49 and 50, the recitation “a third current” is indefinite because the “third current” is not seen in the drawing.

Regarding claim 47, the recitation “feeding a first current...feeding the second current to a load through the transistor while the gate terminal of the transistor is kept at the second potential” is indefinite because it is misdescriptive. Unlike a bipolar transistor, a FET transistor is turned on by applying a potential to its gate. One of ordinary skill in the art knows that with a MOS or FET, there is no gate current. In order to turn a FET transistor ON/OFF, proper potentials, not currents, are applied to its gate. The recitation “the second current” on line 12 is indefinite because it is misdescriptive. The current flowing through the load is not

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the "current" fed to the gate of the transistor. The same rationale is applied to claims 48 and 49.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4, and 47-50 are rejected under U.S.C. 102(e) as being anticipated by Nasu et al. (US 2002/0008543).

Regarding claims 1 and 4, figure 3 of Nasu shows a semiconductor device comprising a transistor (4) electrically connected to load (6) and a circuit (2,11) electrically connected to a gate terminal of the transistor,

wherein the circuit feeds either a first current to the transistor so that the gate terminal of the transistor has a first potential (low) or a second current to the transistor so that the gate terminal of the transistor has a second potential (high), and

wherein the transistor feeds the second current to the load.

Regarding claims 47-50, figure 3 of Nasu shows a method of a semiconductor device comprising the steps of:

feeding a first current to a transistor (4) so that a gate terminal of the transistor has a first potential (low),

feeding a second current to a transistor so that the gate terminal of the transistor has a second potential (high) when capacitor (11) is fully charged, and

feeding the second current to a load through the transistor while the gate terminal of the transistor is kept at the second potential (high). The first current is the charging current so it is larger than the second current. Note that the method of claim 49 is based on the circuit of claim 47.

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nasu et al. (US 2002/0008543).

Regarding claims 2, 5, figure 3 of Nasu includes all the limitations of these claims except for the limitation that the load is a display element. However, the limitations "a display element" is merely intended use thus, they do not further limit the limitations of the claims. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Therefore, these limitations have not been given patentable weight.

Allowable Subject Matter

Claims 7-16, 51 and 52 are allowed.

Claims 7-16 are allowed because the prior art of records (US 2002/0008543) fails to teach or suggest a semiconductor comprising: a load, a constant current source, first, second and third power source lines, first and second transistors and first, second and third switches connected as called for in claim 7.

Claims 51 and 52 are allowed because the prior art of records (US 2002/0008543) fails to teach or suggest a semiconductor comprising a second current source as called for in claim 51.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

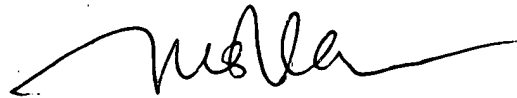
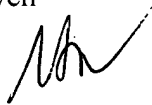
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hiep Nguyen

09-21-06



TUANT.T.LAM
PRIMARY EXAMINER